

IN THE CLAIMS:

Claims 1-23, and 26 have been amended herein. All of the pending claims 1 through 26 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A method for generating a wafer level burn-in reliability curve, comprising:
detecting a signal indicating a transition associated with one of a number m of cycles of burn-in testing of a wafer;
storing a time stamp associated with ~~said~~ the transition in nonvolatile memory in each integrated circuit (IC) die on ~~said~~ the wafer;
performing a built-in self test (BIST) to determine a current number of failures in the each ~~said~~ IC die associated with ~~said~~ the time stamp;
storing ~~said~~ the current number of failures in the each ~~said~~ IC die associated with ~~said~~ the time stamp in ~~said~~ the nonvolatile memory in the each ~~said~~ IC die;
repeating the foregoing for at least one additional cycle of burn-in testing; and
reading ~~said~~ each time stamp ~~and~~ and the current number of failures associated with ~~said~~ the time stamp for each ~~of said~~ at least one additional cycle time stamps.

2. (Currently Amended) The method according to claim 1, wherein ~~said~~ the signal indicating ~~a~~ the transition associated with one of ~~said~~ the number m of cycles of burn-in testing comprises a supervoltage signal.

3. (Currently Amended) The method according to claim 1, wherein ~~said~~ the ~~number m~~ number m of cycles comprises four quarters of burn-in testing.

4. (Currently Amended) The method according to claim 1, wherein ~~said~~ the transition occurs before a first time stamp, between two consecutive time ~~stamps~~ stamps, or after a last time stamp of ~~said~~ the number m of cycles of burn-in testing.

5. (Currently Amended) The method according to claim 1, wherein ~~said~~ the wafer comprises a plurality of integrated circuits.

6. (Currently Amended) The method according to claim 5, wherein each of ~~said~~ the plurality of integrated circuits comprises a memory device.

7. (Currently Amended) The method according to claim 1, wherein ~~said~~ reading ~~said~~ the time stamp ~~and~~ and the current number of failures associated with ~~said~~ the time stamp for each of ~~said~~ time stamps IC die on the wafer comprises reading nonvolatile elements at wafer probe testing.

8. (Currently Amended) The method according to claim 1, further comprising generating ~~said~~ the wafer level burn-in reliability curve from ~~said~~ the time stamp and the each time stamp and ~~said~~ the current number of failures associated with ~~said~~ time stamp for each of said time stamps the one of a number of m cycles and the at least one additional cycle of burn-in testing.

9. (Currently Amended) A method for testing a wafer having integrated circuit (IC) dice formed thereon, comprising:
 stressing ~~said~~ the IC dice;
 storing wafer level burn-in reliability data in nonvolatile elements in each IC die on ~~said~~ the wafer; and
 performing a wafer probe procedure comprising:
 executing a functional test to identify error-free IC dice and repairable IC dice from ~~said~~

the IC dice;
repairing all repairable IC dice; and
reading wafer level burn-in reliability data stored in-~~said~~ the nonvolatile elements.

10. (Currently Amended) The method according to claim 9, wherein ~~said~~ stressing, storing and performing are performed in the order stated.

11. (Currently Amended) The method according to claim 9, wherein ~~said~~ stressing comprises using built-in self-stress circuitry in each IC die.

12. (Currently Amended) The method according to claim 9, further comprising generating burn-in reliability curves from-~~said~~ the wafer level burn-in reliability data.

13. (Currently Amended) The method according to claim 12, further comprising determining whether to scrap-~~said~~ the wafer, to scrap a lot including-~~said~~ the wafer-~~or~~ or to identify a need for additional burn-in.

14. (Currently Amended) The method according to claim 9, wherein ~~said~~ stressing ~~said~~ the IC dice comprises elevating a power supply voltage with respect to a nominal operating voltage.

15. (Currently Amended) The method according to claim 9, further comprising:
forming a sacrificial metal layer for delivering power to-~~said~~ the IC dice on-~~said~~ the wafer prior
to stressing thereof; and
removing-~~said~~ the sacrificial metal layer from-~~said~~ the wafer prior to performing-~~said~~ the wafer
probe procedure.

16. (Currently Amended) A memory device comprising:
a memory array;
address compression circuitry in communication with ~~said~~ the memory array for compressing
memory array addresses into redundancy space;
nonvolatile elements for storing wafer level burn-in data; and
burn-in control circuitry in communication with ~~said~~ the memory array, ~~said~~ the address
compression circuitry and ~~said~~ the nonvolatile elements for controlling wafer level
burn-in and storing wafer level burn-in data in ~~said~~ the nonvolatile elements.

17. (Currently Amended) The memory device according to claim 16, further
comprising signal detection circuitry in communication with ~~said~~ the burn-in control circuitry for
detecting a signal indicating a transition between wafer level burn-in self-stress and self-test
modes.

18. (Currently Amended) The memory device according to claim 17, further
comprising built-in self-stress (BISS) and built-in self-test (BIST) circuitry in communication
with ~~said~~ the nonvolatile elements, ~~said~~ the address compression circuitry, ~~said~~ the burn-in
control circuitry and ~~said~~ the memory array for controlling ~~said~~ the wafer level burn-in self-stress
and self-test modes.

19. (Currently Amended) The memory device according to claim 16, wherein ~~said~~ the
nonvolatile elements comprise antifuse registers.

20. (Currently Amended) The memory device according to claim 16, wherein ~~said~~ the
antifuse registers comprise a number $m + 1$ of n -bit antifuse registers for storing failures detected
before and after m cycles of wafer level burn-in, wherein m and n each comprise positive
integers.

21. (Currently Amended) The memory device according to claim 20, wherein each of ~~said~~ the n -bit antifuse registers comprises one bit for a time stamp and $n - 1$ bits for storing a binary number of failures detected.

22. (Currently Amended) The memory device according to claim 16, wherein ~~said~~ the redundancy space comprises row redundancy space or column redundancy space.

23. (Currently Amended) The memory device according to claim 16, wherein a wafer level burn-in reliability curve may be generated from ~~said~~ the wafer level burn-in data.

24. (Currently Amended) A method for storing numbers of failures detected in an integrated circuit (IC) die on a bulk substrate at discrete time intervals during wafer level burn-in, comprising:

providing nonvolatile elements for storing wafer level burn-in data in ~~said~~ the IC die;

providing built-in self-stress (BISS) circuitry in ~~said~~ the IC die;

providing built-in self-test (BIST) circuitry in ~~said~~ the IC die;

initially testing ~~said~~ the IC die using ~~said~~ the BIST circuitry;

storing a number of failures detected in ~~said~~ the nonvolatile elements;

stressing ~~said~~ the IC die using ~~said~~ the BISS circuitry;

testing ~~said~~ the IC die using ~~said~~ the BIST circuitry; and

repeating as stated above until a predetermined number of cycles of wafer level burn-in are completed.

25. (Original) A method for switching between built-in self-stress (BISS) mode and built-in self-test (BIST) mode in an integrated circuit (IC) during wafer level burn-in, comprising detecting a supervoltage on a nonvolatile programming supply.

26. (Currently Amended) A method of screening unused antifuse registers during wafer level burn-in, comprising reading a time stamp bit for each antifuse register to determine whether the each ~~said~~ antifuse register has been used or has not been used.